CLAIMS

1. (Withdrawn) A method for testing a phase-locked loop (PLL) having a phase-frequency detector (PFD) and a voltage-controlled oscillator (VCO) receiving input from the PFD, the method comprising the steps of:

applying a fixed-level reference clock signal and a test feedback clock signal to the PFD to measure a minimum output frequency of the VCO;

applying a test reference clock signal and a fixed-level feedback clock signal to the PFD to measure a maximum output frequency of the VCO; and

determining lock and capture range of the PLL based on the maximum and minimum frequencies of the VCO.

2. (Withdrawn) The method of Claim 1, further comprising the step of performing a minimal set of tests on the PLL based on the lock and capture range of the PLL.

3. (Withdrawn) The method of Claim 1, wherein the fixed-level reference clock signal is a high-level DC signal.

4. (Withdrawn) The method of Claim 1, wherein the fixed-level reference clock signal is a low-level DC signal.

5. (Withdrawn) The method of Claim 1, wherein the test reference clock signal is a periodic clock signal with a test frequency.

6. (Withdrawn) The method of Claim 1, wherein the test feedback clock signal is generated in response to the test reference clock signal.

7. (Withdrawn) The method of Claim 1, wherein the minimum output frequency of the VCO is measured when the VCO reaches a steady state.

8. (Withdrawn) The method of Claim 1, wherein the maximum output frequency of the VCO is measured when the VCO reaches a steady state.

9. (Withdrawn) An apparatus for testing a phase-locked loop (PLL) having a phase-frequency detector (PFD) and a voltage-controlled oscillator (VCO) receiving input from the PFD, the apparatus comprising:

a switch coupled to the PLL for selectively applying a fixed-level reference clock signal to the PFD while a test feedback clock signal is being applied to the PFD, the VCO generating a minimum output frequency; and

a multiplexer included in the PLL configured for selectively applying a fixed-level feedback clock signal to the PFD while a test reference clock signal is being applied to the PFD, the VCO generating a maximum output frequency.

10. (Withdrawn) The apparatus of Claim 9, further comprising:

a means for determining lock and capture range of the PLL based on the maximum and minimum frequencies of the VCO; and

a means for performing a minimal set of tests on the PLL based on the lock and capture range of the PLL.

11. (Withdrawn) The apparatus of Claim 9, wherein the switch is configured such that the fixed-level reference clock signal is a high-level DC signal.

12. (Withdrawn) The apparatus of Claim 9, wherein the switch is configured such that the fixed-level reference clock signal is a low-level DC signal.

13. (Withdrawn) The apparatus of Claim 9, wherein the switch is configured such that the test reference clock signal is a periodic clock signal with a test frequency.

14. (Withdrawn) The apparatus of Claim 9, wherein the multiplexer is configured such that the test feedback clock signal is generated in response to the test reference clock signal.

15. (Withdrawn) The apparatus of Claim 9, wherein the minimum output frequency of the VCO is measured when the VCO reaches a steady state.

16. (Withdrawn) The apparatus of Claim 9, wherein the maximum output frequency of the VCO is measured when the VCO reaches a steady state.

17. (Original) A method for testing a phase-locked loop (PLL) having a phase-frequency detector (PFD) and a voltage-controlled oscillator (VCO) receiving input from the PFD, the method comprising the steps of:

disabling the PFD;

selectively applying a plurality of test input voltages to the VCO;

measuring output frequencies of the VCO as a function of the test input voltages; and

determining lock and capture range of the PLL based on the measured output frequencies of the VCO as a function of the test input voltages.

18. (Original) The method of Claim 17, further comprising the step of performing a minimal set of tests on the PLL based on the lock and capture range of the PLL.

19. (Original) The method of Claim 17, wherein the test input voltages include discrete DC voltages.

20. (Original) The method of Claim 17, wherein the test input voltages are applied to the VCO through at least one transmission gate.

21. (Currently Amended) An apparatus for testing a phase-locked loop (PLL), the apparatus comprising:

a PLL having a phase-frequency detector (PFD), ~~and~~ a voltage-controlled oscillator (VCO) receiving input from the PFD, and at least one divider receiving input from the VCO; ~~and~~

a test input voltage generator coupled to the VCO for selectively applying a plurality of test input voltages to the VCO while the PFD is disabled; and [[.]]

a frequency measuring module for measuring VCO output frequency via the at least one divider and test clock outputs.

22. (Original) The apparatus of Claim 21, wherein the test input voltage generator comprises:

N resistors coupled in series between supply voltage and ground, the N resistors forming N+1 nodes between the supply voltage and ground, wherein N is an integer greater than or equal to 1;

N+1 switches, each switch being coupled between an input of the VCO and one of the N+1 nodes; and

a test scan signal generator coupled to each of the N+1 switches for controlling the N+1 switches.

23. (Original) The apparatus of Claim 22, wherein the test input voltage generator further comprises a scan-enable switch coupled between the N+1 switches and the input of the VCO, the switch being turned on when the PFD is disabled.

24. (Original) The apparatus of Claim 22, wherein the test scan signal generator generates a plurality of test scan signals for controlling the N+1 switches when the PFD is disabled.

25. (Original) The apparatus of Claim 22, wherein at least one of the N+1 switches includes a transmission gate.

26. (Original) The apparatus of Claim 23, wherein the scan-enable switch includes a transmission gate.

27. (Original) The apparatus of Claim 25, wherein the transmission gate has a p-channel field-effect transistor (PFET) coupled to an n-channel field-effect transistor (NFET).

28. (Original) The apparatus of Claim 26, wherein the transmission gate has a p-channel field-effect transistor (PFET) coupled to an n-channel field-effect transistor (NFET).

29. (Original) The apparatus of Claim 22, wherein the particular test input voltage is determined as follows:

$$V_C = \frac{V_{DD}}{N} * m$$

wherein:

V_C is equivalent to the particular test input voltage;

V_{DD} is equivalent to the supply voltage; and

m is an arbitrary integer between 0 and N including both 0 and N.

30. (Currently Amended) The apparatus of Claim 21, wherein the test input voltage generator comprises:

N resistors coupled in series between the supply voltage and ground or the supply voltage and a lower reference voltage, the N resistors forming N+1 nodes between a supply switch and a

pad, the supply switch connecting the N resistors to the supply voltage when turned on, wherein N is an integer greater than or equal to 1;

N+1 switches, each switch being coupled between an input of the VCO and one of the N+1 nodes; and

a test scan signal generator coupled to each of the N+1 switches for controlling the N+1 switches.

31. (Original) The apparatus of Claim 30, wherein the test input voltage generator further comprises a scan-enable switch coupled between the N+1 switches and the input of the VCO, the switch being turned on when the PFD is disabled.

32. (Original) The apparatus of Claim 30, wherein the test scan signal generator generates a plurality of test scan signals for controlling the N+1 switches when the PFD is disabled.

33. (Original) The apparatus of Claim 30, wherein at least one of the N+1 switches includes a transmission gate.

34. (Original) The apparatus of Claim 31, wherein the scan-enable switch includes a transmission gate.

35. (Original) The apparatus of Claim 33, wherein the transmission gate has a p-channel field-effect transistor (PFET) coupled to an n-channel field-effect transistor (NFET).

36. (Original) The apparatus of Claim 34, wherein the transmission gate has a p-channel field-effect transistor (PFET) coupled to an n-channel field-effect transistor (NFET).

37. (Original) The apparatus of Claim 30, wherein the pad is coupled to ground and the supply switch is turned on, and wherein the particular test input voltage is determined as follows:

$$V_C = \frac{V_{DD} - \alpha}{N} * m$$

wherein:

V_C is equivalent to the particular test input voltage;

V_{DD} is equivalent to the supply voltage;

α is equivalent to a voltage drop across the supply switch when the supply switch is turned on;

m is an arbitrary integer between 0 and N including both 0 and N.

38. (Original) The apparatus of Claim 30, wherein the pad is coupled to an arbitrary input voltage and the supply switch is turned off, and wherein the particular test input voltage is equivalent to the arbitrary input voltage.

39. (Withdrawn) A computer program product for testing a phase-locked loop (PLL) having a phase-frequency detector (PFD) and a voltage-controlled oscillator (VCO) receiving input from the PFD, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer program code for applying a fixed-level reference clock signal and a test feedback clock signal to the PFD to measure a minimum output frequency of the VCO;

computer program code for applying a test reference clock signal and a fixed-level feedback clock signal to the PFD to measure a maximum output frequency of the VCO; and

computer program code for determining lock and capture range of the PLL based on the maximum and minimum frequencies of the VCO.

40. (Withdrawn) The computer program product of Claim 39, further comprising computer program code for performing a minimal set of tests on the PLL based on the lock and capture range of the PLL.

41. (Withdrawn) The computer program product of Claim 39, wherein the fixed-level reference clock signal is a high-level DC signal.

42. (Withdrawn) The computer program product of Claim 39, wherein the fixed-level reference clock signal is a low-level DC signal.

43. (Withdrawn) The computer program product of Claim 39, wherein the test reference clock signal is a periodic clock signal with a test frequency.

44. (Withdrawn) The computer program product of Claim 39, wherein the test feedback clock signal is generated in response to the test reference clock signal.

45. (Withdrawn) The computer program product of Claim 39, wherein the minimum output frequency of the VCO is measured when the VCO reaches a steady state.

46. (Withdrawn) The computer program product of Claim 39, wherein the maximum output frequency of the VCO is measured when the VCO reaches a steady state.